IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A semiconductor device comprising:

a plurality of first wiring structures of a first width which are arranged periodically at first intervals;

a second wiring structure which is formed next to one of the first wiring structures and the lower part of which has a second width substantially equal to the sum of n times the first width of the first wiring structure (n is a positive integer equal to two or more) and (n – 1) times the first interval,

wherein the upper part of the second wiring structure has n convex parts of substantially the first width and (n – 1) concave part.

2. (Cancelled)

3. (Currently Amended) The semiconductor device according to claim 1 [[2]], wherein the (n – 1) concave part has a width substantially equal to the first interval.

4. (Currently Amended) The semiconductor device according to claim 1 [[2]], wherein the second wiring structure is spaced from the one of the first wiring structures substantially at the first interval.

5. (Original) The semiconductor device according to claim 4, wherein the first and second wiring structures form a wiring structure in a memory cell array.

6. (Original) The semiconductor device according to claim 5, wherein the first wiring structures constitute memory cells and the second wiring structure constitutes a select gate configured to select the memory cells.

7. (Original) The semiconductor device according to claim 6, wherein the first wiring structures constitute a memory cell unit of a NAND memory cell array.

8. (Original) The semiconductor device according to claim 7, wherein each of the first wiring structures comprises:

a first insulating film above a semiconductor substrate;

a first conductive film above the first insulating film;

a second insulating film above the first conductive film;

a second conductive film above the second insulating film; and

a third insulating film above the second conductive film.

9. (Previously Presented) The semiconductor device according to claim 8, wherein the second wiring structure comprises:

the first insulating film;

the first conductive film above the first insulating film;

the second conductive film above the first conductive film; and

the third insulating film above the second conductive film.

10. (Original) The semiconductor device according to claim 9, wherein the second conductive film is formed in contact with the first conductive film in the second wiring structure.

11. (Original) The semiconductor device according to claim 10, wherein the second wiring structure further includes the second insulating film between the first conductive film and the second conductive film.

12-20 (Cancelled)

21. (New) A semiconductor device comprising:

a plurality of first wiring structures of a first width which are arranged periodically at first intervals; and

a second wiring structure which is formed next to one of the first wiring structures,

wherein the upper part of the second wiring structure has n convex parts of substantially the first width (n is a positive integer equal to two or more) and (n – 1) concave part.

22. (New) The semiconductor device according to claim 21, wherein the lower part of the second wiring structure has a second width substantially equal to the sum of n times the first width of the first wiring structure and (n – 1) times the first interval.

23. (New) The semiconductor device according to claim 22, wherein the (n – 1) concave part has a width substantially equal to the first interval.

24. (New) The semiconductor device according to claim 22, wherein the second wiring structure is spaced from the one of the first wiring structures substantially at the first interval.

25. (New) The semiconductor device according to claim 24, wherein the first and second wiring structures form a wiring structure in a memory cell array.

26. (New) The semiconductor device according to claim 25, wherein the first wiring structures constitute memory cells and the second wiring structure constitutes a select gate configured to select the memory cells.

27. (New) The semiconductor device according to claim 26, wherein the first wiring structures constitute a memory cell unit of a NAND memory cell array.

28. (New) The semiconductor device according to claim 27, wherein each of the first wiring structures comprises:

a first insulating film above a semiconductor substrate;

a first conductive film above the first insulating film;

a second insulating film above the first conductive film;

a second conductive film above the second insulating film; and

a third insulating film above the second conductive film.

29. (New) The semiconductor device according to claim 28, wherein the second wiring structure comprises:

the first insulating film;

the first conductive film above the first insulating film;

the second conductive film above the first conductive film; and

the third insulating film above the second conductive film.

30. (New) The semiconductor device according to claim 29, wherein the second conductive film is formed in contact with the first conductive film in the second wiring structure.

31. (New) The semiconductor device according to claim 30, wherein the second wiring structure further includes the second insulating film between the first conductive film and the second conductive film.